# Dynamic Response of Amorphous In-Ga-Zn-O Thin-Film Transistors for 8K×4K Flat-Panel Display

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Amorphous In-Ga-Zn-O thin-film transistor (a-IGZO TFT) is viewed as an important future thin-film device candidate for next-generation ultra-high resolution flat-panel displays and image sensors [1]. Although extensive studies were conducted on a-IGZO TFTs electrical properties including their electrical instabilities [2], there are no reports on TFT dynamic characteristics. From literature it is clear that the TFT dynamic measurements are critical for design optimization of the AM-OLEDs [3] and AM-LCDs [4]. The dynamic characteristics allow to evaluate TFT charging performance including the switching speed of liquid-crystal cells (LCs) and the presence of level-shift voltage induced a DC offset voltage across the LCs which might cause image sticking or flickering problems. In this paper, for the first time, we report on the dynamic characteristics of the bottom-gate a-IGZO TFTs. Experiment results obtained for a-IGZO TFT are compared to conventional hydrogenated amorphous silicon (a-Si:H) TFTs.

To measure dynamic response, we have designed and fabricated integrated testing circuits, where a single a-IGZO TFT was connected to a storage capacitor. [3] Figure 1 shows the top view image and schematic cross-section of integrated testing circuit used in this study. The bottom-gate back-channel-etching (BCE) a-IGZO TFT is fabricated on glass substrate using 4 photo-lithography masks with a gate-to-source/drain overlap length of 4μm. The current-voltage (I-V) characteristics of the TFT are measured by Agilent B1500A Semiconductor Analyzer. Figure 2 shows the measured $I_d$-$V_{gs}$ and $I_d$-$V_{ds}$ characteristics of a-IGZO TFT: $I_{off}<10^{-12}$A, $V_{TH}$=6.0V, $R_{ds}\approx$0.1MΩ and $\mu_{eff}$=5.62cm$^2$/V·s.

To study dynamic response, we developed the dynamic measurements set up. [3] A two-channel pulse generator, HP 8110A, is used to apply operational testing signals: one channel is set to be single-pulse mode applying high/low level data voltage on drain electrode of TFT and another channel set to be double-pulse mode (one for set and another for reset, see Fig. 3) applying gate voltages on bottom gate electrode. A picoprobe (HP18C-1-5-HV, GGB Inc.), with an extremely low input capacitance (≤0.02pF) and high impedance is used to measure the voltage response at source electrode. Agilent MSO7104B mixed-signal oscilloscope is used to monitor and record all signals during the dynamic operation. Figure 3 shows one example of operational testing signals and measured voltage response. The tested circuit contains an IGZO TFT with W/L=75/4(μm) and storage capacitor of $C_{ST}$=1.8pF. Extracted from Fig. 3, the level-shift voltage for our device is less than 0.6V and the time constant (τ) is 180ns, which is close to value estimated by $\tau=R_{ds}\times C_{ST}$ (~178ns). The charging time is then calculated by $t_{CH}=3\times\tau$ (time required to charge the capacitor up to 95%$V_{DH}$), which is equal to 0.54μs. The a-IGZO TFT appears to be much faster than conventional a-Si:H TFTs, see Table I. From these results we can conclude that a-IGZO TFTs can be used for very high resolution displays, such as 8K×4K, where a-Si:H TFT is not suitable.

Finally, different testing circuits were fabricated to investigate the impacts of TFT channel width (W) and storage capacitance ($C_{ST}$) on the dynamic response. Figure 4 shows the measured variation of charging time ($t_{CH}$) and level-shift voltage ($\Delta V_P$) with different TFT channel widths and storage capacitances. In all cases, TFT channel width-length ratios (W/L)s are set to be 10:1; high/low level values of data voltages are set to be $V_{DH}/V_{DL}$=10V/0V and high/low level values of gate voltages are set to be $V_{GH}/V_{GL}$=18V/-2V. From Fig.4 (a), we observed that both $\Delta V_P$ and $t_{CH}$ increase with the increasing TFT channel width. Results indicate that for a given W/L, smaller W will result in a shorter charging time and less level-shift voltage. Moreover, storage capacitances also influence $\Delta V_P$ and $t_{CH}$: $\Delta V_P$ decreases with the increasing $C_{ST}$ while $t_{CH}$ increases, as shown in Fig. 4 (b). These results are very important for design of future ultra-high resolution displays and image sensors.

[1] G. Yoo, et al., **Sensors and Actuators A**, vol. **158**. pp. 280 - 283, (2010).
[2] T. Kamiya et al., **Sci. Technol. Adv. Mater.**, vol. **11**, pp.1-23 (2010).
[3] H. Lee et al., **IEEE Trans. Elev. Dev.**, vol. **55**, pp. 2338-2347 (2008).
[4] N. Nakagawa et al., **SID 92 DIGEST**, pp. 781-784 (1992).

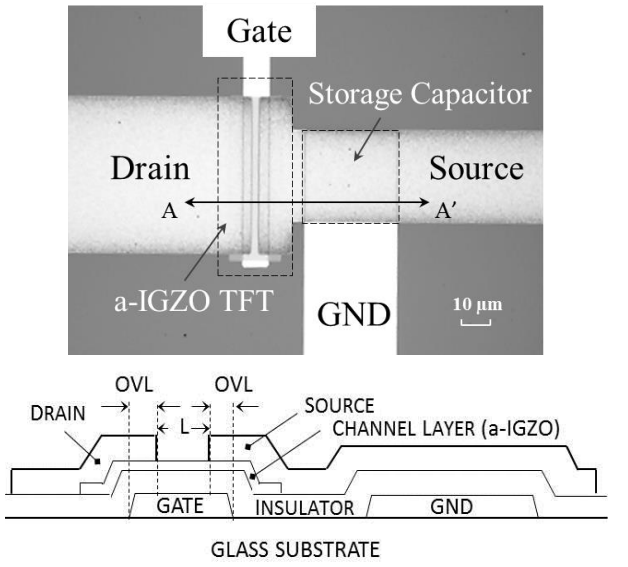


Fig.1. Top view (top) and schematic cross-section (bottom) of the a-IGZO TFT and storage capacitor integrated testing circuit fabricated at University of Michigan.

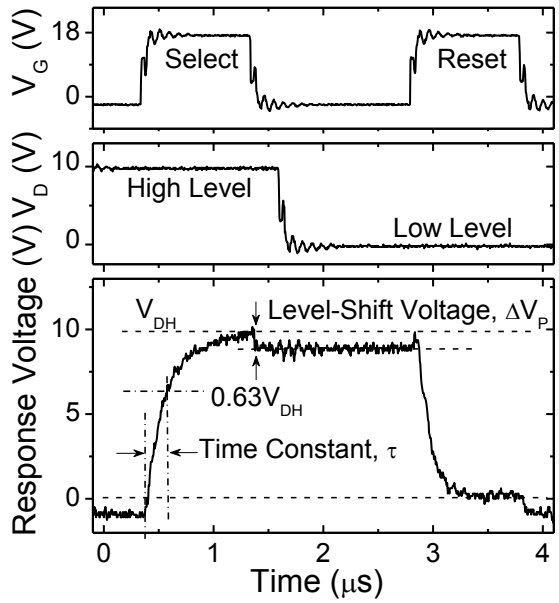


Fig.3. Experimental 1MHz dynamic response of a-IGZO TFT: Tested integrated circuit contains a-IGZO TFT with W/L=75/4 (μm) and a capacitor of 1.78pF.

Table I. Dynamic Response for a-Si:H and a-IGZO TFTs

| TFT | $\Delta V_P$ (V) | $t_{CH}$ (μs) | W/L (μm) | OVL (μm) | $C_{ST}$ (pF) |
|---|---|---|---|---|---|
| a-Si:H [3] | 2.3 | 7.2 | 1000/10 | 4 | 20 |
| a-IGZO | 0.6 | 0.54 | 75/4 | 4 | 1.8 |

[1] $V_{DH}/V_{DL}$=10V/0V; $V_{GH}/V_{GL}$=20V/-5V

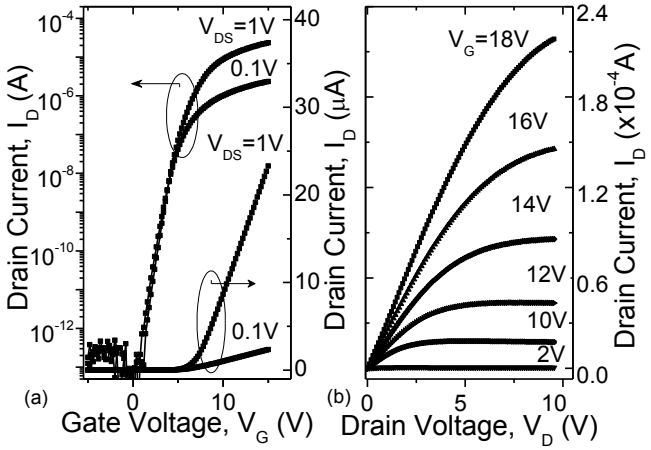


Fig.2. Id-Vg (a) and $I_{ds}$-$V_{ds}$ (b) characteristics of a-IGZO TFT: $I_{off}$<$10^{-12}$A, $V_{th}$=6V, on/off ratio>$10^7$, $R_{on}$≈0.1MΩ and $\mu_{eff}$=5.62cm$^2$/V·s. a-IGZO TFT device has a dimension of W/L=75/4 (μm) and gate-to-source overlap length of 4μm.

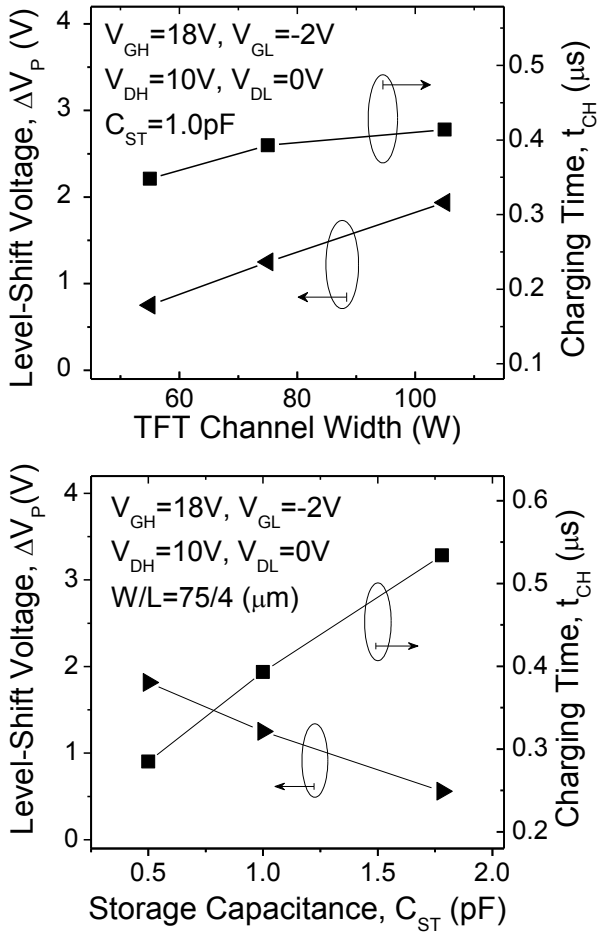


Fig.4. Impacts of integrated storage capacitance and TFT dimensions (W/L) on the a-IGZO TFTs dynamic characteristics: level-shift voltage and charging time properties.